|   | Туре | L # | Hits  | Search Text   | DBs  |
|---|------|-----|-------|---|--|
| 1 | BRS  | L2  | 2012  | (channel near region)<br>near25 (gate near<br>dielectric)   | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 2 | BRS  | L3  | 60106 | "1" and (remov\$3) near15<br>(sidewall\$1 or side near<br>wall\$1 or spacer\$1)                       | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 3 | BRS  | L4  | 507   | 2 and (remov\$3) near15<br>(sidewall\$1 or side near<br>wall\$1 or spacer\$1)                         | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 4 | BRS  | L5  | 153   | 2 and ((substrate) near35<br>(remov\$3) near15<br>(sidewall\$1 or side near<br>wall\$1 or spacer\$1)) | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |

|   | Туре | L #        | Hits | Search Text   | DBs  |
|---|------|------------|------|---|--|
| 5 | BRS  | L6         | 0    | (channel near region) near25 (gate near dielectric) near25 (gate near3 mandrel) | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 6 | BRS  | <b>L</b> 7 | 0    | (channel near region) near25 (gate near dielectric) near25 (mandrel)            | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 7 | BRS  | L8         | 1    | (channel near region)<br>near25 (gate) near25<br>(mandrel)                      | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 8 | BRS  | L9         | 114  | (gate near3 mandrel)  | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |

|    | Туре | L#  | Hits | Search Text  | DBs  |
|----|------|-----|------|--|--|
| 9  | BRS  | L10 | 19   |  | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 10 | BRS  | L11 | 0    | (gate near3 mandrel) near25<br>(side near wall\$1) | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 11 | BRS  | L12 | 1231 | (mandrel) near25 (side near<br>wall\$1)            | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 12 | BRS  | L13 | 2585 | (mandrel) near25 (spacer\$1<br>or sidewall\$1)     | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |

|    | Туре | L # | Hits | Search Text   | DBs  |
|----|------|-----|------|---|--|
| 13 | BRS  | L14 | 74   |   | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 14 | BRS  | L15 | 92   | 13 and ((source or drain) near (region))                                | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |
| 15 | BRS  | L16 | 41   | 13 and ((source) near (region))   | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD   |
| 16 | BRS  | L17 | 16   | (fill\$3) near35 ((gate near<br>dielectric) near5 (side or<br>plat\$1)) | US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B |

|   | U | 1 | Document ID          | Title  |
|---|---|---|----------------------|--|
| 1 |   |   | US 20050009305<br>A1 | METHOD OF FORMING FREESTANDING<br>SEMICONDUCTOR LAYER  |
| 2 |   |   | US 20020109179<br>A1 | SELF-ALIGNED NON-VOLATILE<br>RANDOM ACCESS MEMORY CELL AND<br>PROCESS TO MAKE THE SAME                                     |
| 3 |   |   | US 20020028554<br>A1 | Formulation of multiple gate oxides thicknesses without exposing gate oxide or silicon surface to photoresist              |
| 4 |   |   | US 20020011608<br>A1 | Self aligned method of forming a semiconductor memory array of floating gate memory cells, and a memory array made thereby |
| 5 |   |   | US 6593177 B2        | Self aligned method of forming a semiconductor memory array of floating gate memory cells, and a memory array made thereby |
| 6 |   |   | US 6552378 B1        | Ultra compact DRAM cell and method of making   |
| 7 |   |   | US 6525371 B2        | Self-aligned non-volatile random access memory cell and process to make the same   |
| 8 |   |   | US 6344381 B1        | Method for forming pillar CMOS   |

|    | Ü | 1 | Document   | ID | Title   |
|----|---|---|------------|----|---|
| 9  |   |   | US 6339001 | В1 | Formulation of multiple gate oxides thicknesses without exposing gate oxide or silicon surface to photoresist                         |
| 10 |   |   | US 6329685 |    | Self aligned method of forming<br>a semiconductor memory array<br>of floating gate memory cells<br>and a memory array made<br>thereby |
| 11 |   |   | US 6255699 | B1 | Pillar CMOS structure   |

|    | U | 1 | Document   | ID | Title  |
|----|---|---|------------|----|--|
| 12 |   |   | US 6252267 | B1 | Five square folded-bitline<br>DRAM cell  |
| 13 |   |   | US 6100123 | Α  | Pillar CMOS structure  |
| 14 |   |   | us 6090660 |    | Method of fabricating a gate<br>connector  |
| 15 |   |   | US 6037620 | A  | DRAM cell with transfer device extending along perimeter of trench storage capacitor |
| 16 |   |   | US 5893735 | Α  | Three-dimensional device<br>layout with sub-groundrule<br>features                   |

|    | บ | 1 | Document   | ID | Title  |
|----|---|---|------------|----|--|
| 17 |   |   | US 4833094 |    | Method of making a dynamic ram cell having shared trench storage capacitor with sidewall-defined bridge contacts and gate electrodes |
| 18 |   |   | US 4785337 |    | Dynamic ram cell having shared trench storage capacitor with sidewall-defined bridge contacts and gate electrodes                    |
| 19 |   |   | US 5893735 |    | Three dimensional cell forming process for dynamic random access memory (DRAM)   |